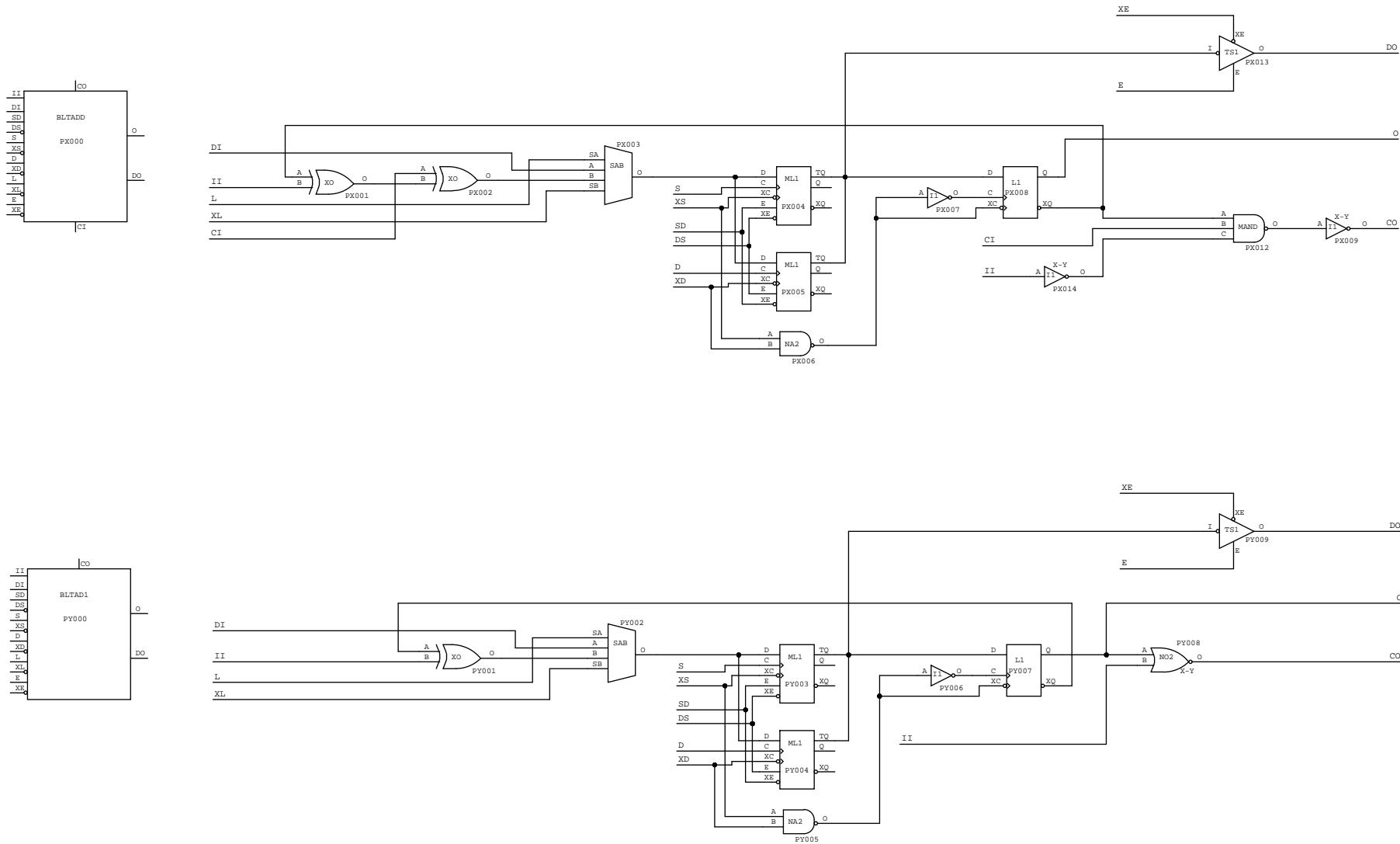
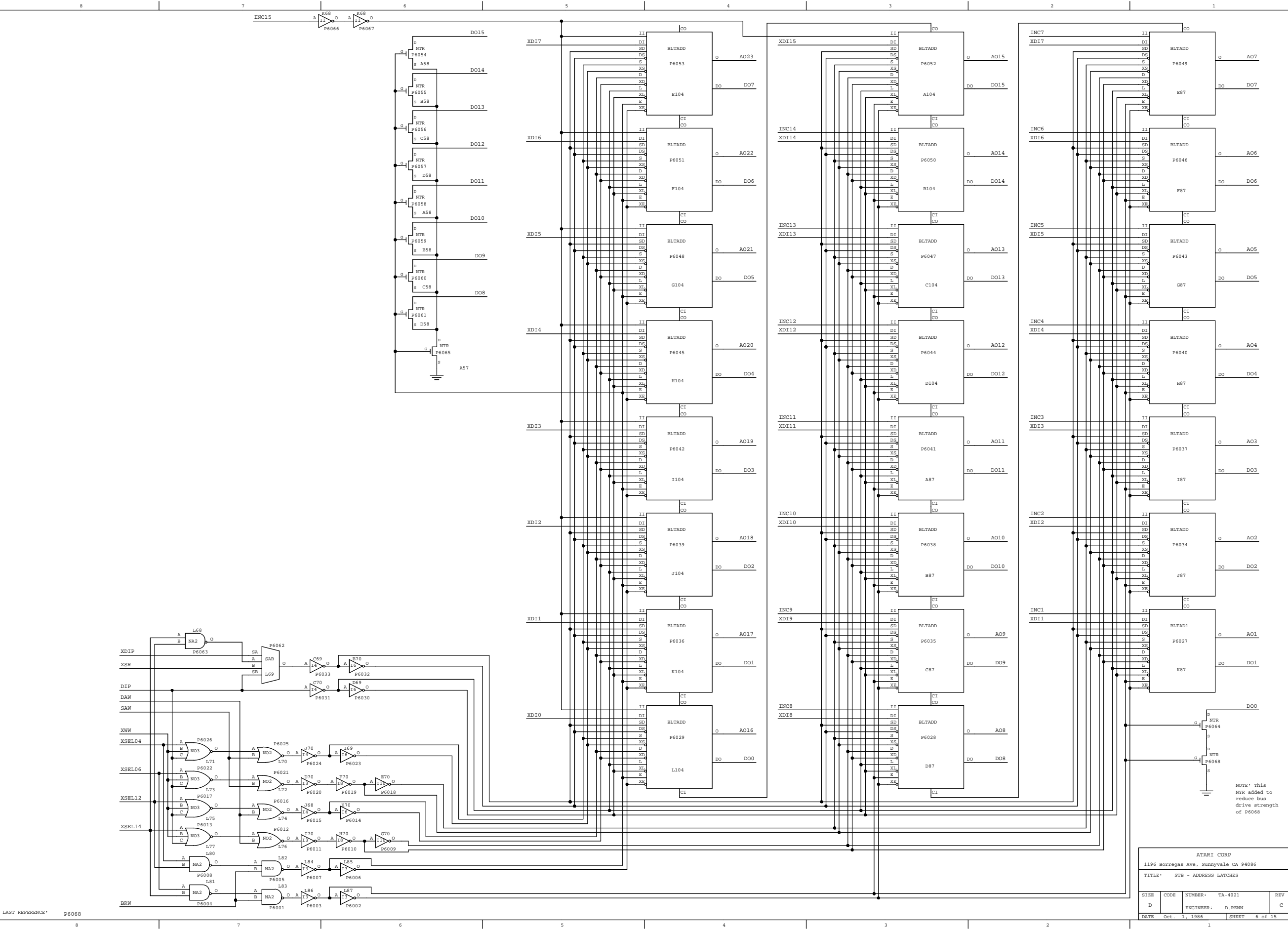


NOTE: This design was modified to buffer the DO output and invert the O output. The DO output went from a TG to a TS1. This prevents data bus loading from affecting the operation of the BLT cell, and speed up the read cycle timing. The O output was inverted so that a subsequent inverter on the same line on page 8 could also be removed. This will save 1.5*23 gates, and will speed up the address bus response by a few nanoseconds.

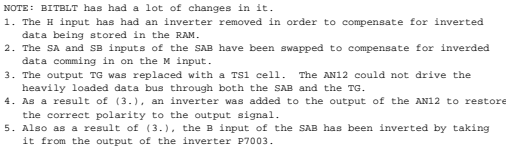
NOTE #2: This design was again modified to compensate for the inversion of the INC and DI inputs. The inverters added above were removed, which fixed the DI input. And the XO was converted to an XN for the INC input. However, the XN of th output of an XN with a third number is the same as the XO to the output of an XO and the third number. Therefore, all of the XN's have been removed.



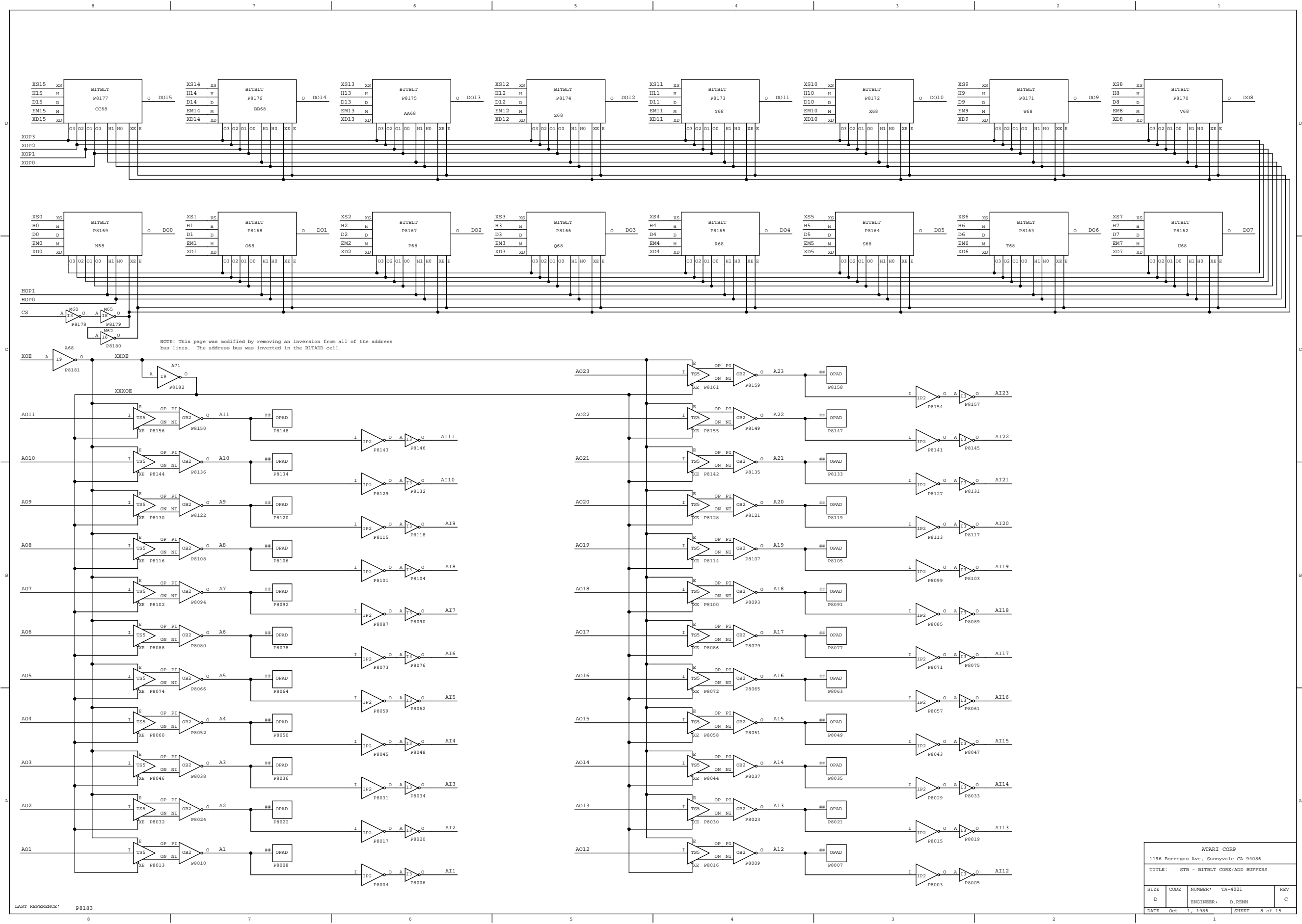


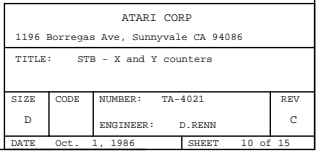
LAST REFERENCE: P6068

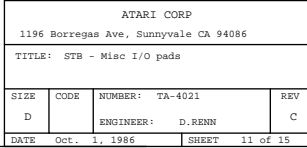
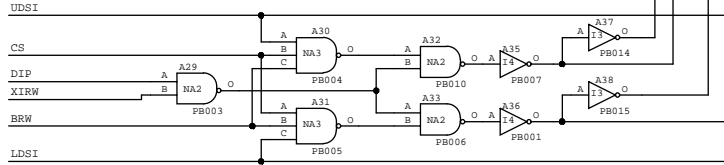
ATARI CORP				
1196 Borregas Ave, Sunnyvale CA 94086				
TITLE: STB - ADDRESS LATCHES				
SIZE	CODE	NUMBER:	TA-4021	REV
D		ENGINEER:	D.RENN	C
DATE	Oct. 1, 1986	SHEET	6 of 15	

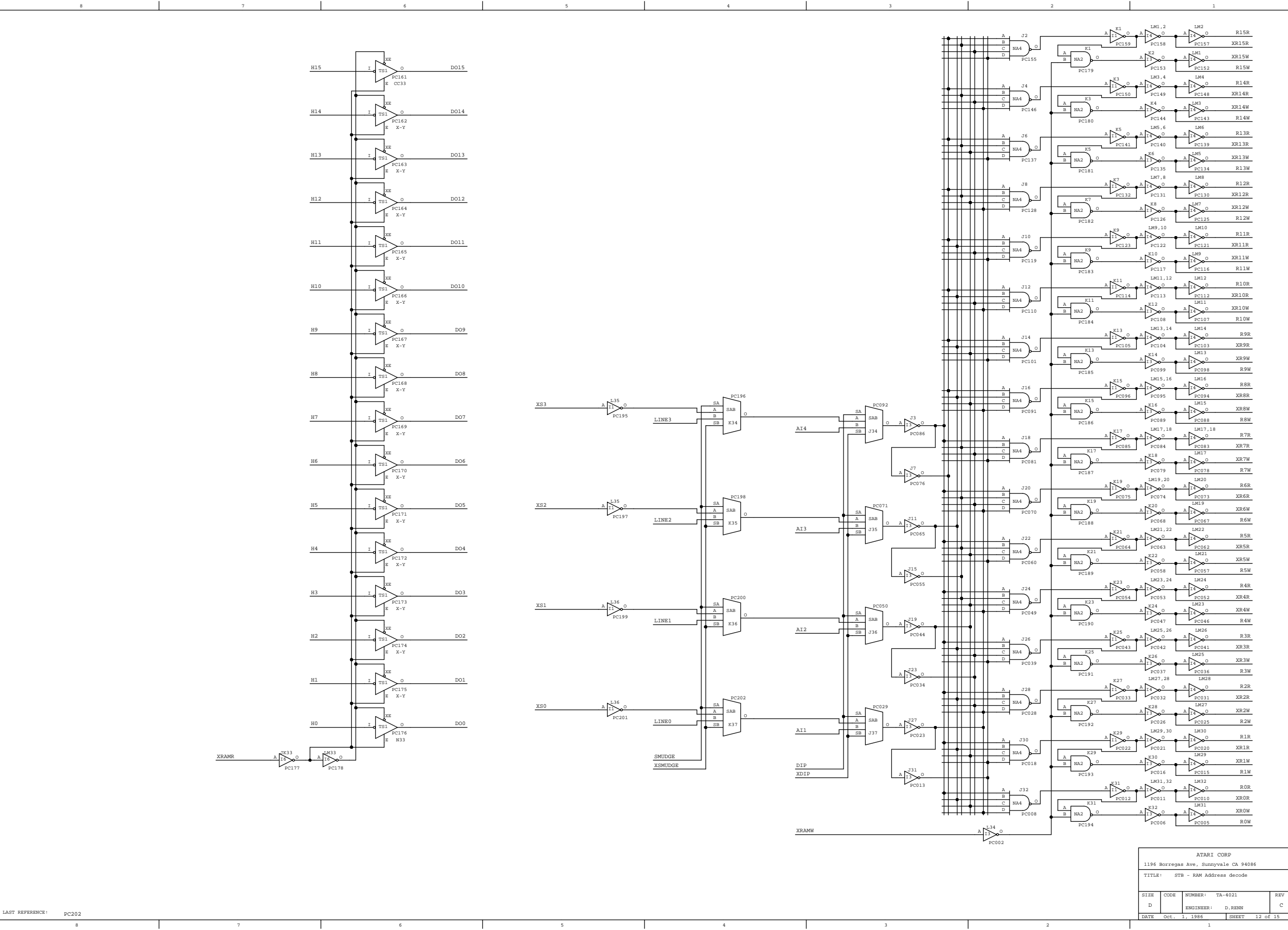


ATARI CORP			
1196 Borregas Ave, Sunnyvale CA 94086			
TITLE: BITBLT CELL DEFINITION			
SIZE	CODE	NUMBER: TA-4021	REV
D		ENGINEER: D.RENN	C
DATE	Oct. 1, 1986		SHEET 7 of 15



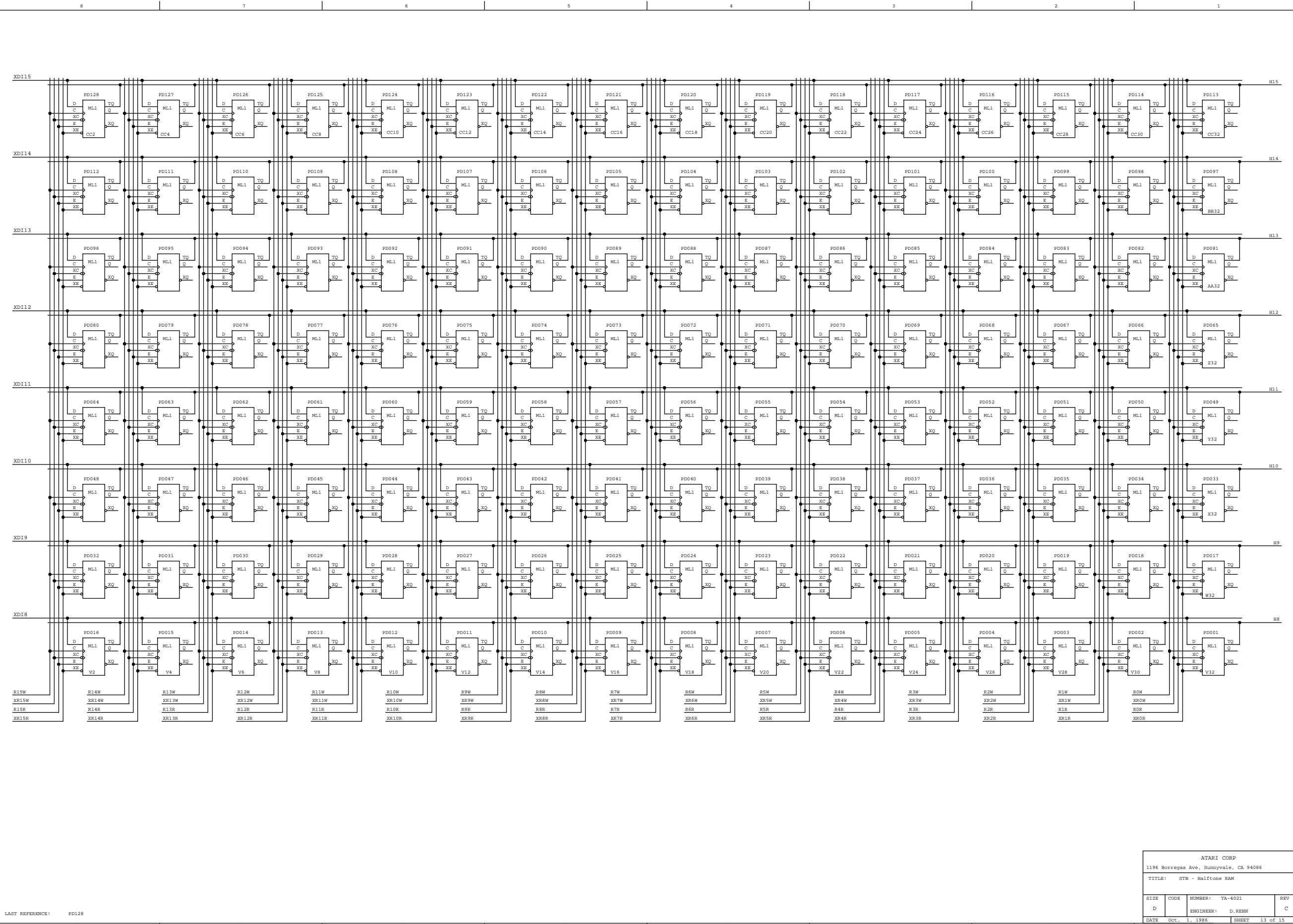






LAST REFERENCE: PC202

ATARI CORP				
1196 Borregas Ave, Sunnyvale CA 94086				
TITLE: STB - RAM Address decode				
SIZE	CODE	NUMBER:	TA-4021	REV
D		ENGINEER:	D.RENN	C
DATE	Oct. 1, 1986	SHEET 12 of 15		



LAST REFERENCE: PD128

ATARI CORP				
1196 Borregas Ave, Sunnyvale, CA 94086				
TITLE: STB - Halftone RAM				
SIZE	CODE	NUMBER:	TA-4021	REV
D		ENGINEER:	D.RENN	C
DATE	Oct. 1, 1986			SHEET 13 of 15



LAST REFERENCE: PE128

ATARI CORP				
1196 Borregas Ave, Sunnyvale, CA 94086				
TITLE: STB - Halftone RAM				
SIZE	CODE	NUMBER:	TA-4021	REV
D		ENGINEER:	D.RENN	C
DATE	Oct. 1, 1986	SHEET	14 of 15	

